**REMARKS**

Claims 1-35 and 37-39 remain pending in the application, with claims 1-29 and 34 having been withdrawn from consideration and only remaining claims 30-33, 35 and 37-39 being examined. Claims 30 and 39 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

The drawings received by the Office on 24 November 2004 are objected to as allegedly failing to comply with 37 CFR §1.84(p)(5). More particularly, the Office states that "Replacement Figures 13, 14, 15, 16, 17, 18, 19, 21, 22, 26, 28, and 29 are acceptable", but objects that "Replacement Figure 1 does not show the changes indicated on the Annotated Marked-Up Figure 1."

This objection is not understood. The basis for the original objection to Figure 1 was that it included reference numbers "1" and "2", which are not mentioned in the specification. In Applicants' previously-filed response, this objection was addressed by amending Figure 1 so as to remove the reference signs identified in the Office Action. An Annotated Marked-Up Figure 1 was provided to illustrate that the two reference signs were being removed (indicated in red by means of a "curly-cue" circle surrounding those parts of the figure that were being removed). A Replacement Sheet was also supplied, showing a clean version of the amended figure (i.e., with the reference numbers "1" and "2" as well as their associated lead lines removed). So far as the Applicants can tell, the original objection to Figure 1 was completely addressed by the previously filed amended figures.

The Office now objects to Figure 1, first stating that "The drawings are objected to ... because they do not include the following reference sign(s) mentioned in the description: ...." However, the Office does not identify which reference signs are alleged to be missing. Consequently, Applicants have no basis for addressing the Office's expressed concern.

The Office then goes on to state that "Replacement Figure 1 does not show the changes indicated on the Annotated Marked-Up Figure 1." This statement is simply wrong, since the marked-up figure shows which two reference numbers and which two lead lines are being removed, and the Replacement Sheet depicts the original version of the figure minus the two indicated reference numbers and lead lines.

For the foregoing reasons, it is respectfully requested that the objection to the figures be withdrawn. If the Office intends to make a new objection to Figure 1, it is requested that

the Office expressly state what it believes is missing from the figure, or alternatively, what it sees in the figure that it believes should be removed.

Claims 30, 31, 33, 35, and 39 again stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over "The Universal Serial Bus Specification", Revision 1.0 ("USB") in view of IEEE Standard 1394-1995 ("IEEE-1394"), US Patent Number 4,709,364 to Hasegawa et al. ("Hasegawa"), and US Patent Number 6,230,226 to Hu et al. ("Hu"). These rejections are respectfully traversed.

In responding to Applicants' previously-filed arguments pointing out that the prior art lacks the requisite suggestion or motivation to make the various combinations of references, the Office again argues, *inter alia*, that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the bus system of USB with the arbitration requests of IEEE-1394, ... , because USB and IEEE-1394 are both commonly used serial bus protocols; ...." Applicants respectfully question how the fact that the USB bus system and the IEEE-1394 bus system were commonly used *as separate bus systems* adds any support to the Office's argument that the skilled artisan would have derived from their teachings the necessary motivation to combine their various aspects into a new bus system. To the extent that the Office is implying that it would have been obvious to try different combinations of features from these separate bus systems, the Office is reminded that "whether a particular combination might be 'obvious to try' is not a legitimate test of patentability." *In re Fine*, 5 USPQ2d 1596, 1599 (Fed. Cir. 1988).

Furthermore, in response to Applicants' previously filed arguments addressing these rejections, the Office now states, *inter alia*, that "[i]n response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which Applicant relies (i.e., the bus is a pipelined packet switched bus) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. ... The Examiner further notes that there are no limitations in the claims requiring a pipeline bus that does not allow circulating empty packets."

In order to expedite prosecution of the application, independent claims 30 and 39 have each been amended, without introduction of new matter, to specifically recite "wherein the bus is a pipelined packet switched bus that does not allow circulating empty packets".

Accordingly, the Office should now give these features patentable weight when reconsidering the following arguments.

It is well settled that establishing a *prima facie* case of obviousness requires that three basic criteria be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP §2143, p. 2100-129 (Rev. 2, 2004).

In the present instance, the Office has failed to make out a *prima facie* case of obviousness against claims 30-33, 35, and 37-39 at least because neither the references relied upon in the rejection nor the knowledge generally available to one of ordinary skill in the art provide any suggestion or motivation to make the combination of their respective teachings. Instead, the Office has engaged in an impermissible hindsight analysis, "us[ing] the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). The Court of Appeals for the Federal Circuit has stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Furthermore, the references relied upon in the rejection relate to different types of bus architectures, so that one of ordinary skill in the art would not have had the requisite reasonable expectation of success in making the combination now suggested by the Office.

These and other arguments are elaborated upon in the following discussion.

Various embodiments of the invention are concerned with bus access to a bus provided on an integrated circuit. In the embodiments defined by the claims, the bus is a pipelined packet switched bus. In one aspect, two types of arbitration are used: central arbitration is used to allocate timeslots in response to specific requests from agents connected to the bus, and distributed arbitration is used to allow bus access by agents on an ad hoc basis using empty timeslots.

Accordingly, independent claim 30 defines an integrated circuit for a computer system comprising a bus architecture; a plurality of modules connected to the bus architecture; and an arbitration unit for granting access to the bus in response to requests

received from the modules, the granting of access being in the form of a dedicated packet issued from the arbitration unit, whereby only the module which has been granted access can use that particular dedicated packet to gain access to the bus. The integrated circuit is characterized in that "the arbitration unit is operable to issue empty packets during periods when the bus is idle, the empty packets being usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet." As mentioned above, claim 30 has now been amended to expressly recite "wherein the bus is a pipelined packet switched bus that does not allow circulating empty packets." (Emphasis added.)

Independent claim 39 defines a method of granting bus access to a module in an integrated circuit for a computer system comprising a plurality of modules interconnected by the bus, and an arbitration unit for granting access to the bus by issuing dedicated packets in response to requests received from the modules. As stated in claim 39, the method comprises "issuing empty packets from the arbitration unit during periods when the bus is idle; and allowing any module to use the empty packet in order to gain access to the bus." Also as mentioned above, claim 39 has also now been amended to expressly recite "wherein the bus is a pipelined packet switched bus that does not allow circulating empty packets." (Emphasis added.)

In rejecting claims 30-33, 35, and 37-39, the Office relies in part on the USB reference, but acknowledges that this reference at least fails to "teach that the arbitration unit grants access to the bus in response to requests received from the modules; and that the arbitration unit is operable to issue empty packets during periods when the bus is idle, the empty packets being usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet."

To make up for these deficiencies of the USB reference, the Office relies in part on IEEE-1394 for its teaching of "an arbitration unit granting access to the bus in response to requests received from the modules," but here acknowledges that IEEE-1394 also fails to disclose at least "sending an empty packet during periods when the bus is idle that are usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet." To make up for this last missing piece of the puzzle, the Office further relies on Hasegawa as teaching "sending an empty packet during periods when the

bus is idle that are usable by a module to gain access to the bus without making a specific request to the arbitration unit for a dedicated packet."

The Office's reliance on this combination of references is unfounded because the USB and 1394 documents disclose serial system buses, which are not suitable for use on an integrated circuit. Both systems make use of a global arbitration system which operates to allow or disallow access by all of the agents connected to the bus at the same time. Such techniques are simply not applicable to a packet switched pipeline bus, as used in embodiments of the present invention, and as now expressly defined in the claims.

Moreover, the Hasegawa document concerns a token ring packet switched system which has no central arbitration system. In Hasegawa, access to the bus is controlled by the use of empty packets circulating in the ring which are picked up by agents requiring access to the bus. The techniques used in Hasegawa are not applicable to a pipeline bus embodying the subject matter defined by claims 30 and 39, since such a pipeline bus does not allow circulating empty packets. (As noted above, each of claims 30 and 39 has been amended to further define "a pipelined packet switched bus that does not allow circulating empty packets" as a claim feature.) No such central arbitration is possible in the Hasegawa disclosure, since using central arbitration would mean that the ring is broken, or that each agent would be connected to the arbiter independently of one another. Such independent connection would defeat the object of the token ring scheme which is intended to minimize the number of connections.

In making its rejection, the Office uses the approach of starting with the USB document and adding teachings from the IEEE 1394 and Hasegawa documents to derive the invention. However, there is simply no suggestion or motivation provided in any of these references to combine their teachings because all three documents are not relevant to on-chip pipelined buses, and, furthermore, the Hasegawa document is not relevant to the USB and IEEE 1394 documents. It is therefore inconceivable that the person of ordinary skill would have combined Hasegawa with either of the other two documents. Hasegawa does not make use of central arbitration, and USB and IEEE 1394 do not use free packets for ad hoc arbitration. The teachings of these three documents would simply not be combined by one of ordinary skill in the art.

Even assuming that the Office were to maintain that the three documents could be theoretically combined, this would be impossible for one of ordinary skill in the art for the

following reasons. Starting with the serial system bus of USB, the Office admits that this disclosure teaches neither the provision of access to the bus in response to requests nor the use of empty packets to allow ad hoc bus access. Although it is not suggested by these references, combining the access on request feature from IEEE 1394 with USB might be possible, since both documents relate to serial system bus designs using global arbitration.

However, Hasegawa proposes control of a token ring network which makes no use of global arbitration, but rather uses a system in which connected agents seize available time slots. There is simply no suggestion that the teaching of Hasegawa is appropriate for use in a serial system bus such as described in USB/IEEE 1394. There is no equivalent mechanism in USB to which to apply the teaching of Hasegawa. To be able to apply such teaching it would be necessary to provide packet switching and timeslot allocation. It is respectfully submitted that such provision goes far beyond normal design practice for one of ordinary skill in the art.

The Office considers the disclosures to be relevant to "on-chip" buses because there are examples of USB controllers "on-chip". (See the Office's argument in paragraph 11 of the Action, made with respect to now-canceled claim 36.) However, the controller simply allows an IC to communicate with an external bus, and the provision of the bus itself on an IC is not a trivial modification. The USB/1394/Hasegawa buses are not intended or appropriate for an on-chip usage. It is believed that the Office's new reliance on the Hu reference does not make up for this deficiency because Hu is understood to merely disclose a USB controller "on-chip."

In USB and IEEE 1394, the arbitration decision is final; no further access is allowed outside of the arbiter's control. In contrast, the present invention allows subsequent ad hoc access, outside of the direct control of the arbiter.

For at least the foregoing reasons, independent claims 30 and 39 are patentably distinguishable over the USB, 1394, Hasegawa, and Hu documents, regardless of whether these documents are considered individually or in any combination. Claims 31, 33, and 35 each depend from independent claim 30, and are therefore patentable for at least the reasons set forth above with respect to that base claim. Therefore, it is respectfully requested that the rejection of claims 30, 31, 33, 35 and 39 under Section 103 be withdrawn.

Claim 32 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, Hasegawa, and Hu as applied to claim 30, and further in view of US Patent Number 5,400,334 to Hayssen ("Hayssen"). Claim 37 was rejected under 35 U.S.C. §103(a)

as allegedly being unpatentable over USB, IEEE-1394, Hasegawa, and Hu as applied to claim 30, and further in view of US Patent Number 5,912,710 to Fujimoto ("Fujimoto"). Claim 38 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over USB, IEEE-1394, Hasegawa, and Hu as applied to claim 30, and further in view of US Patent Number 5,986,644 to Herder et al. ("Herder"). These rejections are respectfully traversed.

Claims 32, 37, and 38 each depend from independent claim 30, and are therefore patentably distinguishable over the prior art of record at least for the reasons set forth above with respect to that base claim. Therefore, it is respectfully requested that the rejection of these claims under Section 103 be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
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Date: May 2, 2005

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I hereby certify that this correspondence is being sent via facsimile transmission (703-872-9306) to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 2, 2005.

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